#11
BA 12/16/03

D E C L A R A T I O N



I, Hiroshi Kurokawa, residing at 7th FL., SHUWA KIOICHO PARK BLDG., 3-6, KIOICHO, CHIYODA-KU, TOKYO, JAPAN, hereby declare that I have a thorough knowledge of Japanese and English languages, and that the attached pages contains a correct translation into English of the application document of Japanese Patent Application No. 9-313432 filed on November 14, 1997, in the name of CANON KABUSHIKI KAISHA.

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statement were made with the knowledge that willful false statements and the like so made, are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signed this 1st day of December, 2003

H. Kurokawa

Hiroshi Kurokawa

RECEIVED
DEC 1 0 2003
Technology Center 2600

Translation of Japanese Patent Application No. 9-313432

| | |
|---|---|
| [Type of Document(s)] | Application for patent |
| [Reference Number] | 3574006 |
| [Filing Date] | November 14, 1997 |
| [Addressee] | Director-General of the Patent Office, Esq. |
| [International Patent Classification] | H04N 5/00 |
| [Title of Invention] | PHOTOELECTRIC CONVERSION DEVICE, CONTROL METHOD THEREOF, FOCUS DETECTION DEVICE, AND STORAGE MEDIUM |
| [Number of Claim(s)] | 20 |
| [Inventor] | |
| [Address/Domicile] | c/o Canon Kabushiki Kaisha 30-2, Shimomaruko 3-chome, Ohta-ku, Tokyo, Japan |
| [Name] | Tatsuyuki Tokunaga |
| [Applicant for Patent] | |
| [Identification Number] | 000001007 |
| [Name] | Canon Kabushiki Kaisha |
| [Agent] | |
| [Identification Number] | 100090273 |
| [Patent Attorney] | |
| [Name] | Takayoshi Kokubun |
| [Telephone Number] | 03-3590-8901 |
| [Detail of Fee(s)] | |
| [Register Number of Prepayment] | 035493 |
| [Amount of Payment] | 21000 |
| [List of Attached Documents] | |
| [Classification] | Specification 1 |
| [Classification] | Drawing(s) 1 |
| [Classification] | Abstract 1 |
| [Number of General Power of Attorney] | 9705348 |

[Type of the Document] Specification

[Title of the Invention] PHOTOELECTRIC CONVERSION DEVICE, CONTROL METHOD THEREOF, FOCUS DETECTION DEVICE, AND STORAGE MEDIUM

[What Is Claimed Is:]

[Claim 1] A photoelectric conversion device characterized by comprising:

photoelectric conversion means including a photoelectric conversion element constructed by a plurality of pixels, and storage means for storing predetermined control information; and

control means for controlling charge accumulation of said photoelectric conversion means on the basis of the control information stored in said storage means.

[Claim 2] The photoelectric conversion device according to claim 1, characterized in that said photoelectric conversion means further includes monitor means for monitoring and outputting an accumulated charge state in said photoelectric conversion element, and

said control means includes selection means for selecting an arbitrary one of a plurality of pieces of status information on the basis of the control information stored in said storage means, and comparison means for comparing an output from said monitor means with the status information selected by

said selection means, and controls the charge accumulation of said photoelectric conversion means on the basis of a comparison result of said comparison means.

[Claim 3] A photoelectric conversion device characterized by comprising:

photoelectric conversion means including a photoelectric conversion element constructed by a plurality of pixels, and storage means for storing predetermined control information;

read means for amplifying an accumulated charge signal of said photoelectric conversion element with a predetermined amplification factor, and reading out the amplified signal; and

control means for controlling the amplification factor of said read means on the basis of the control information stored in said storage means.

[Claim 4] The photoelectric conversion device according to claim 3, characterized in that said photoelectric conversion means further includes monitor means for monitoring and outputting an accumulated charge state in said photoelectric conversion element, and

said control means includes selection means for selecting an arbitrary one of a plurality of pieces of status information on the basis of the control information stored in said storage means, and

comparison means for comparing an output from said monitor means with the status information selected by said selection means, and controls the amplification factor of said read means on the basis of a comparison result of said comparison means.

[Claim 5] The photoelectric conversion device according to claim 1 or 3, characterized by comprising a plurality of photoelectric conversion means equivalent to said photoelectric conversion means.

[Claim 6] The photoelectric conversion device according to claim 2 or 4, characterized in that said monitor means monitors and outputs information based on a maximum accumulated charge amount of said photoelectric conversion element.

[Claim 7] The photoelectric conversion device according to claim 2 or 4, characterized in that said control means stores the status information selected by said selection means in said storage means as the control information.

[Claim 8] The photoelectric conversion device according to claim 1 or 3, characterized in that said photoelectric conversion means is constructed by forming said photoelectric conversion element and storage means on a single substrate.

[Claim 9] The photoelectric conversion device according to claim 1 or 3, characterized in that said control means includes determination means for

determining predetermined information on the basis of an accumulated charge signal read out from said photoelectric conversion means, and stores the information determined by said determination means in said storage means as the control information.

[Claim 10] A control method of controlling charge accumulation of a photoelectric conversion element constructed by a plurality of pixels, characterized by comprising

a control step of reading out control information from a memory corresponding to the photoelectric conversion element, and controlling the charge accumulation of the photoelectric conversion element on the basis of the control information.

[Claim 11] The control method according to claim 10, characterized in that the control step includes:

a monitor output step of monitoring and outputting an accumulated charge state in the photoelectric conversion element;

a selection step of selecting an arbitrary one of a plurality of pieces of status information on the basis of the control information read out from the memory;

a comparison step of comparing a monitor output in the monitor output step with the status information selected in the selection step; and

an accumulation control step of controlling the

charge accumulation of the photoelectric conversion element on the basis of a comparison result in the comparison step.

[Claim 12] The control method according to claim 10, characterized in that the control step includes a step of controlling charge accumulation operations of a plurality of photoelectric conversion elements equivalent to the photoelectric conversion element on the basis of control information in a plurality of memories formed in correspondence with the plurality of photoelectric conversion elements.

[Claim 13] A control method of controlling operation for reading out an accumulated charge signal from a photoelectric conversion element constructed by a plurality of pixels while applying the signal with a predetermined amplification factor, characterized by comprising

a control step of reading out control information from a memory corresponding to the photoelectric conversion element, and controlling the amplification factor on the basis of the control information.

[Claim 14] The control method according to claim 13, characterized in that the control step includes:

a monitor output step of monitoring and outputting an accumulated charge state in the photoelectric conversion element;

a selection step of selecting an arbitrary one of

a plurality of pieces of status information on the basis of the control information read out from the memory;

a comparison step of comparing a monitor output in the monitor output step with the status information selected in the selection step; and

an amplification factor control step of controlling the amplification factor on the basis of a comparison result in the comparison step.

[Claim 15] The control method according to claim 13, characterized in that the control step includes a step of controlling the amplification factors of accumulated charge signals read out from a plurality of photoelectric conversion elements equivalent to the photoelectric conversion element on the basis of control information in a plurality of memories formed in correspondence with the photoelectric conversion elements.

[Claim 16] The control method according to claim 11 or 14, characterized in that the monitor output step includes a step of monitoring and outputting information based on a maximum accumulated charge amount of the photoelectric conversion element.

[Claim 17] The control method according to claim 11 or 14, characterized in that the control step includes a step of storing the status information selected in the selection step in the memory as the

control information.

[Claim 18] The control method according to claim 10 or 13, characterized in that the control step includes a determination step of determining predetermined information on the basis of an accumulated charge signal read out from the photoelectric conversion means, and a storage step of storing the information determined in the determination step in the memory as the control information.

[Claim 19] A focus detection device characterized by including a photoelectric conversion device of any one of claims 1 to 9.

[Claim 20] A storage medium characterized by computer-readably storing processing steps of a control method of any one of claims 10 to 18.

[Detailed Description of the Invention]

[0001]

[Technical Field to Which the Invention Belongs]

The present invention relates to a photoelectric conversion device applied to photographing equipment such as a still camera, video camera, and the like, various observation apparatuses, and the like, its control method, a focus detection device, and a storage medium which computer-readably stores processing steps of implementing the control method of the photoelectric conversion device and focus detection device.

[0002]

[Prior Art]

Conventionally, various types of so-called auto-focus (AF) cameras, which detect the focus state of an object, and automatically focus on the object by changing the moving distance of the photographing lens in correspondence with the detected focus state, have been proposed.

Such AF cameras and the like use the method of detecting the focus state by, e.g., forming an object image on a photoelectric conversion element (to be referred to as a sensor hereinafter) formed by a plurality of photoelectric conversion pixels (to be simply referred to as pixels hereinafter), and performing predetermined arithmetic processing for a plurality of pixel signals output from the sensor.

In this method, in order to accurately detect the focus states of objects having various luminance levels (e.g., from a high-luminance object to low-luminance one), the amplification factor (to be referred to as a gain hereinafter) upon reading signals, and the charge accumulation time of the sensor must be appropriately controlled.

This is because if the level of an image signal of an object formed by a plurality of pixel signals (to be referred to as a video signal hereinafter) is too high, it exceeds the dynamic range of a pixel signal

that can be processed by the apparatus, and the video signal becomes different from an actual one, thus impairing precision. By contrast, if the level of the video signal is too low, noise components increase relatively, and may impair precision.

[0003]

Fig. 8 shows a photoelectric converter 500 which controls the read gain of pixel signals and the charge accumulation time in a sensor 54.

[0004]

The photoelectric converter 500 comprises the sensor 54 constructed by a plurality of pixels, a peak detection circuit 53 for detecting and outputting a maximum accumulated charge amount during charge accumulation on the sensor 54, a memory 52 for receiving and holding pixel signals upon completion of charge accumulation on the sensor 54, a counter 55, a level output circuit 56 for outputting a level value selected from a plurality of level values in accordance with the count value of the counter 55, a comparator 57 for comparing the outputs from the level output circuit 56 and peak detection circuit 53, and outputting the comparison result, and a read amplifier 58 for outputting the pixel signals held in the memory 52 with the gain corresponding to the count value of the counter 55.

[0005]

Note that the respective units of the photoelectric converter 500 are controlled by a controller 51, which especially controls charge accumulation on the sensor 54.

[0006]

More specifically, as shown in Fig. 9, the controller 51 outputs a reset signal rst to the sensor 54 and counter 55 (step S501).

In response to this signal, charges on all the pixels of the sensor 54 are initialized, and the counter 55 is reset to an initial value "0" (count = 0).

After that, charge accumulation on the sensor 54 is actually started.

[0007]

Subsequently, the controller 51 sets its internal timer (not shown) at an initial value "0" (timer = 0), thus starting time measurement of the charge accumulation (step S502).

[0008]

The controller 51 checks if the timer value timer of the internal timer has exceeded a maximum accumulation time Etime (step S503).

If "timer ≧ Etime", the controller 51 determines the end of charge accumulation, and outputs a signal trans indicating this to the sensor 54. In response to this signal, charges accumulated on the individual

pixels of the sensor 54 are transferred as pixel signals to the memory 52, thus ending charge accumulation on the sensor 54 (step S508).

[0009]

On the other hand, if "timer < Etime" in step S503, the controller 51 checks if an output signal comp from the comparator 57 is "1", i.e., if an output signal c_level of the level output circuit 56 is larger than an output signal p_out of the peak detection circuit 53 (step S504).

If "comp ≠ 1", the flow returns to step S503 to repeat the subsequent processing steps.

[0010]

Note that the output signal c_level of the level output circuit 56 will be described in detail later.

[0011]

If "comp = 1" in step S504, the controller 51 checks if the timer value timer of the internal timer has exceeded an intermediate accumulation time Htime (step S505).

As a result of checking, if "timer ≧ Htime", the flow advances to step S508, thus ending charge accumulation on the sensor 54.

[0012]

If "timer < Htime" in step S505, the comparator 51 checks if the count value count of the counter 55 is "3" (step S506).

If "count = 3", the flow advances to step S508, thus ending charge accumulation on the sensor 54.

[0013]

If "count ≠ 3" in step S506, the controller 51 outputs a signal up_c to the counter 55. In response to this signal, the count value count of the counter 55 is counted up (step S507).

After that, the flow returns to step S503 to repeat the subsequent processing steps.

[0014]

Charge accumulation control of the sensor 54 is done in this way, and the read of pixel signals held in the memory 52 after completion of charge accumulation is controlled by a signal shift output from the controller 51.

With this control, pixel signals s_out read out from the memory 52 are multiplied by the gain by the read amplifier 58, and are output from an output terminal Vout.

At this time, the read amplifier 58 multiplies the pixel signals s_out from the memory 52 by the gain in accordance with the count value count of the counter 55.

[0015]

The charge accumulation time of the sensor 54 is controlled by switching the output signal c_level of the level output circuit 56.

The charge accumulation time and the output signal c_level of the level output circuit 56 will be described below with reference to Figs. 10(A) and 10(B).

[0016]

In the following description, assume that the level output circuit 56 has four level values "level1.0" to "level1.3", and selectively outputs one of these level values in accordance with the count value count of the counter 55.

In Figs. 10(A) and 10(B), the abscissa plots the charge accumulation time, and the ordinate plots the values of the output signal c_level of the level output circuit 56 and the output signal p_out of the peak detection circuit 53.

Fig. 10(A) shows a case wherein the object is relatively bright, and the peak output of each pixel signal, i.e., the output signal p_out of the peak detection circuit 53 rises quickly. Fig. 10(B) shows, contrary to Fig. 10(A), a case wherein the object is relatively dark, and the peak output of each pixel signal rises slowly.

[0017]

(Case of Fig. 10(A))

When charge accumulation is started, since the count value count of the counter 55 is initialized (step S501), the output signal c_level of the level

output circuit 56 changes to "levell.0".

When the charge accumulation time (timer value timer of the internal timer) has reached "A-1", the output signal p_out of the peak detection circuit 53 exceeds the output signal c_level of the level output circuit 56. As a result, when the output signal comp of the comparator becomes "1", the count value count of the counter 55 is counted up (steps S503 to S507). Since the counted-up count value count is supplied to the level output circuit 56, the output signal c_level of the level output circuit 56 changes to "levell.1".

Similarly, when the charge accumulation time has reached "A-2", the count value count of the counter 55 is counted up, and the output signal c_level of the level output circuit 56 changes to "levell.2".

Also, when the charge accumulation time has reached "A-3", the count value count of the counter 55 is counted up, and the output signal c_level of the level output circuit 56 changes to "levell.3".

When the charge accumulation time has reached "A-4", since the count value count of the counter 55 is "3", charge accumulation on the sensor 54 ends (the flow advances to step S508 as a result of checking in step S506).

[0018]

(Case of Fig. 10(B))

When the charge accumulation time has reached

"B-1" and "B-2", the count value count of the counter 55 is counted up, and the output signal c_level of the level output circuit 56 changes from "level1.0" to "level1.1" and from "level1.1" to "level1.2", in the same manner as in "A-1" to "A-3" mentioned above.

When the charge accumulation time has reached "A-3", if it has exceeded the intermediate accumulation time due to the slowly rising output signal p_out of the peak detection circuit 53, charge accumulation on the sensor 54 ends (the flow advances to step S508 as a result of checking in step S506).

[0019]

In this way, by switching the output signal c_level of the level output circuit 56 among four levels, the charge accumulation time is controlled in correspondence with the object condition, e.g., so that a sufficiently long charge accumulation time is assured when the object is light, or the charge accumulation time is prevented from becoming excessively long when the object is dark.

[0020]

The gain of the read amplifier 58 is controlled in accordance with the count value count of the counter 55, and as a consequence, since the gain of the read amplifier 58 is controlled in accordance with the peak output (p_out) of each pixel signal, pixel signals can always be read out while effectively using the dynamic

range of pixel signals that can be processed by the apparatus.

[0021]

[Problems That the Invention Is to Solve]

However, when the aforementioned conventional photoelectric converter 500 is applied to a multi-point AF camera which can effect the AF function at a plurality of distance measurement points, the arrangement including the comparator 57 and the like shown in Fig. 8 must be provided for each of all the distance measurement points. As a result, the circuit scale becomes huge, and the area of an IC chip increases.

[0022]

In order to solve such problem, a method of dividing a single sensor into regions in units of distance measurement points, and controlling the charge accumulation time by a single controller while sequentially scanning the respective regions is proposed.

With this method, multi-point AF can be realized by a reasonable chip size while suppressing an increase in IC chip area.

[0023]

However, in this method, when a pixel signal is read out from each region and is then compared to control the charge accumulation time of the region

(sensor) of each distance measurement point, it is intermittently checked for a certain region during charge accumulation if charge accumulation is to end.

When such method is used in the photoelectric converter 500 shown in Fig. 8, since the output signal c_level of the level output circuit 56 is "level1.0" immediately after the beginning of charge accumulation, the count value count of the counter 55 becomes "3" for a high-luminance object which makes the output signal p_out of the peak detection circuit 53 rise rapidly, and charge accumulation ends. For this reason, much time is required, and the charge accumulation time cannot be appropriately controlled. As a result, since the level of the video signal of an object exceeds the dynamic range, the obtained image may be distorted.

[0024]

The present invention has been made to overcome the above drawbacks, and has as its object to provide a photoelectric conversion device which can always perform appropriate charge accumulation control independently of the object types to read pixel signals by effectively using the dynamic range, can attain accurate auto-focus, and can realize them without increasing the circuit scale and cost, its control method, a focus detection device, and a storage medium which computer-readably stores processing steps of implementing the control method of the photoelectric

conversion device.

[0025]

[Means of Solving the Problems]

Under the object, the first invention is characterized by comprising photoelectric conversion means including a photoelectric conversion element constructed by a plurality of pixels, and storage means for storing predetermined control information, and control means for controlling charge accumulation of the photoelectric conversion means on the basis of the control information stored in the storage means.

[0026]

According to the first invention, the second invention is characterized in that the photoelectric conversion means further includes monitor means for monitoring and outputting an accumulated charge state in the photoelectric conversion element, and the control means includes selection means for selecting an arbitrary one of a plurality of pieces of status information on the basis of the control information stored in the storage means, and comparison means for comparing an output from the monitor means with the status information selected by the selection means, and controls the charge accumulation of the photoelectric conversion means on the basis of a comparison result of the comparison means.

[0027]

The third invention is characterized by comprising photoelectric conversion means including a photoelectric conversion element constructed by a plurality of pixels, and storage means for storing predetermined control information, read means for amplifying an accumulated charge signal of the photoelectric conversion element with a predetermined amplification factor, and reading out the amplified signal, and control means for controlling the amplification factor of the read means on the basis of the control information stored in the storage means.

[0028]

According to the third invention, the fourth invention is characterized in that the photoelectric conversion means further includes monitor means for monitoring and outputting an accumulated charge state in the photoelectric conversion element, and the control means includes selection means for selecting an arbitrary one of a plurality of pieces of status information on the basis of the control information stored in the storage means, and comparison means for comparing an output from the monitor means with the status information selected by the selection means, and controls the amplification factor of the read means on the basis of a comparison result of the comparison means.

[0029]

According to the first or third invention, the fifth invention is characterized by comprising a plurality of photoelectric conversion means equivalent to the photoelectric conversion means.

[0030]

According to the second or fourth invention, the sixth invention is characterized in that the monitor means monitors and outputs information based on a maximum accumulated charge amount of the photoelectric conversion element.

[0031]

According to the second or fourth invention, the seventh invention is characterized in that the control means stores the status information selected by the selection means in the storage means as the control information.

[0032]

According to the first or third invention, the eighth invention is characterized in that the photoelectric conversion means is constructed by forming the photoelectric conversion element and storage means on a single substrate.

[0033]

According to the first or third invention, the ninth invention is characterized in that the control means includes determination means for determining predetermined information on the basis of an

accumulated charge signal read out from the photoelectric conversion means, and stores the information determined by the determination means in the storage means as the control information.

[0034]

The 10th invention is a control method of controlling charge accumulation of a photoelectric conversion element constructed by a plurality of pixels, characterized by comprising a control step of reading out control information from a memory corresponding to the photoelectric conversion element, and controlling the charge accumulation of the photoelectric conversion element on the basis of the control information.

[0035]

According to the 10th invention, the 11th invention is characterized in that the control step includes a monitor output step of monitoring and outputting an accumulated charge state in the photoelectric conversion element, a selection step of selecting an arbitrary one of a plurality of pieces of status information on the basis of the control information read out from the memory, a comparison step of comparing a monitor output in the monitor output step with the status information selected in the selection step, and an accumulation control step of controlling the charge accumulation of the

photoelectric conversion element on the basis of a comparison result in the comparison step.

[0036]

According to the 10th invention, the 12th invention is characterized in that the control step includes a step of controlling charge accumulation operations of a plurality of photoelectric conversion elements equivalent to the photoelectric conversion element on the basis of control information in a plurality of memories formed in correspondence with the plurality of photoelectric conversion elements.

[0037]

The 13th invention is a control method of controlling operation for reading out an accumulated charge signal from a photoelectric conversion element constructed by a plurality of pixels while applying the signal with a predetermined amplification factor, characterized by comprising a control step of reading out control information from a memory corresponding to the photoelectric conversion element, and controlling the amplification factor on the basis of the control information.

[0038]

According to the 13th invention, the 14th invention is characterized in that the control step includes a monitor output step of monitoring and outputting an accumulated charge state in the

photoelectric conversion element, a selection step of selecting an arbitrary one of a plurality of pieces of status information on the basis of the control information read out from the memory, a comparison step of comparing a monitor output in the monitor output step with the status information selected in the selection step, and an amplification factor control step of controlling the amplification factor on the basis of a comparison result in the comparison step.

[0039]

According to the 13th invention, the 15th invention is characterized in that the control step includes a step of controlling the amplification factors of accumulated charge signals read out from a plurality of photoelectric conversion elements equivalent to the photoelectric conversion elements on the basis of control information in a plurality of memories formed in correspondence with the photoelectric conversion elements.

[0040]

According to the 11th or 14th invention, the 16th invention is characterized in that the monitor output step includes a step of monitoring and outputting information based on a maximum accumulated charge amount of the photoelectric conversion element.

[0041]

According to the 11th or 14th invention, the 17th

invention is characterized in that the control step includes a step of storing the status information selected in the selection step in the memory as the control information.

[0042]

According to the 10th or 13th invention, the 18th invention is characterized in that the control step includes a determination step of determining predetermined information on the basis of an accumulated charge signal read out from the photoelectric conversion means, and a storage step of storing the information determined in the determination step in the memory as the control information.

[0043]

In the 19th invention, a focus detection device is characterized by including a photoelectric conversion device of any one of claims 1 to 9.

[0044]

In the 20th invention, a storage medium is characterized by computer-readably storing processing steps of a control method of any one of claims 10 to 18.

[0045]

[Embodiments]

Embodiments of the present invention will be described hereinafter with reference to the accompanying drawings.

[0046]

(1) First Embodiment

[0047]

A photoelectric conversion device according to the present invention is realized by, e.g., a photoelectric conversion device 100 shown in Fig. 1.

[0048]

The photoelectric conversion device 100 is capable of multi-point AF, and comprises a controller 1, a plurality of sensor array blocks $2_1$ to $2_n$, a level output circuit 3, a buffer 4 with a selection signal, a comparator 5, and a read amplifier 6, as shown in Fig. 1.

[0049]

The plurality of sensor array blocks $2_1$ to $2_n$ are set in correspondence with a plurality of distance measurement points (to be referred to as regions 1 to n hereinafter), and have the same arrangement.

For example, the sensor array block $2_1$ corresponding to region 1 of regions 1 to n comprises analog switches $11_1$ and $12_1$, a buffer $13_1$ with a selection signal, a memory $14_1$, a peak detection circuit $15_1$, a sensor $16_1$, and a RAM $17_1$.

[0050]

The building units of the photoelectric conversion device 100 will be explained below.

[0051]

(Controller 1)

The controller 1 corresponds to control means, and performs operation control of the overall device and, especially, charge accumulation control of the sensor array blocks $2_1$ to $2_n$.

As will be described in detail later, the controller 1 has a program memory 18 which pre-stores a processing program for performing various kinds of control operations, and when the processing program stored in the program memory 18 is read out and executed by the controller 1, the operation control of the overall device as well as charge accumulation control is executed.

[0052]

(Sensor Array Blocks $2_1$ to $2_n$)

The sensor array blocks $2_1$ to $2_n$ correspond to photoelectric conversion means.

For example, in the sensor array block $2_1$, the sensor $16_1$ comprises a pair of sensor arrays for phase difference detection, and forms the first image by around 30 to 80 pixels, and the second image by the same number of pixels.

[0053]

The peak detection circuit $15_1$ corresponds to monitor means. The circuit $15_1$ detects the maximum accumulated charge amount (the output value of a pixel that exhibits the highest output) during charge

accumulation of the sensor $16_1$, and outputs it to the analog switch $12_1$.

At this time, when the analog switch $12_1$ is ON in response to a signal psel_1 from the controller 1, an output signal p_out from the peak detection circuit $15_1$ is output to one input terminal ("+" terminal) of the comparator 5 via the analog switch $12_1$.

[0054]

The memory $14_1$ temporarily holds charges accumulated on the sensor $16_1$ as pixel signals simultaneously with the end of charge accumulation on the sensor $16_1$.

At this time, when the analog switch $11_1$ is ON in response to a signal sel_1 from the controller 1, since a signal shift output from the controller 1 is supplied to the memory $14_1$, pixel signals s_out held on the memory $14_1$ are sequentially output to the input terminal of the read amplifier 6 via the analog switch $11_1$.

[0055]

The RAM $17_1$ corresponds to storage means, and serves as a memory for storing information (control information) associated with charge accumulation on the sensor $16_1$. Upon reception of a signal ltcR_1 from the controller 1, the RAM $17_1$ stores the value of a signal Rin from the level output circuit 3 (to be described later).

When the controller 1 supplies a signal rsel_1 to the buffer $13_1$ with a selection signal, an output signal Ro from the RAM $17_1$ is output as a signal r_out via the buffer $13_1$ with a selection signal. The output signal r_out is supplied to the read amplifier 6 and level output circuit 3. Note that the signal r_out is 2-bit data.

[0056]

Since the remaining sensor array blocks $2_2$ to $2_n$ have the same arrangement as that of the aforementioned sensor array block $2_1$, a detailed description thereof will be omitted.

[0057]

(Level Output Circuit 3)

The level output circuit 3 corresponds to selection means or determination means, and comprises three resistors r_1, r_2, and r_3, four analog switches 21 to 24, an amplifier 25, a decoder 26, a selector 27, and a counter 28, as shown in, e.g., Fig. 2. The selector 27 receives a signal r_out selectively output from the sensor array blocks $2_1$ to $2_n$ (e.g., in the sensor array block $2_1$, the signal r_out output from the RAM $17_1$ via the buffer $13_1$ with a selection signal), and an output signal c_level of the amplifier 25 and an output signal c_out of the counter 28 determine the outputs from the level output circuit 3. Note that the output signal c_out is 2-bit data.

[0058]

In such level output circuit 3, the three resistors r_1, r_2, and r_3 are inserted between two reference potentials vref1 and vref2, and voltage-divide the two reference potentials vref1 and vref2 into four voltage values (level values as status information) level1.3, level1.2, level1.1, and level1.0, which are output in correspondence with the analog switches 21 to 24.

At that time, one of the analog switches 21 to 24 is turned on depending on the output from the decoder 26, and only the output from the ON analog switch is output to the input terminal of the amplifier 25. In this way, one of the four level values level1.3, level1.2, level1.1, and level1.0 is selected, and the selected level value is output as a signal c_level from the amplifier 25.

[0059]

The decoder 26 selects one of the four analog switches 21 to 24 in accordance with an output signal sel_out from the selector 27, and outputs a signal for turning on the selected analog switch. Note that the output signal sel_out is 2-bit data.

[0060]

The selector 27 selects one of an output signal c_out from the counter 28 and the signal r_out selectively output from the sensor array blocks $2_1$ to

$2_n$ upon reception of a signal sel_level from the controller 1, and outputs the selected signal as the signal sel_out to the decoder 26.

[0061]

The counter 28 initializes its count value to "0" upon reception of a signal rst_level from the controller 1, and increments its count value upon reception of a signal G_up from the controller 1. The count value of the counter 28 serves as the signal c_out.

Note that a signal max_level supplied from the controller 1 to the counter 28 will be explained later.

[0062]

(Buffer 4 with Selection Signal)

The buffer 4 with a selection signal receives the signal c_out (the count value of the counter 28) from the level output circuit 3, and outputs the signal c_out as a signal Rin to be written in the RAMs $17_1$ to $17_n$ of the sensor array blocks $2_1$ to $2_n$ upon reception of a signal W_ram from the controller 1.

[0063]

(Comparator 5)

The comparator 5 corresponds to comparison means, and receives the signal c_level (the output from the amplifier 25) from the level output circuit 3, and a signal p_out selectively output from the sensor array blocks $2_1$ to $2_n$ (e.g., in the sensor array block $2_1$, a

signal p_out output from the peak detection circuit $15_1$ via the analog switch $12_1$). The comparator 5 compares the signals c_level and p_out, and outputs the comparison result as a signal comp to the controller 1.

Note that the output signal comp from the comparator 5 is set at "1" when the signal p_out is larger than the signal c_level.

[0064]

The read amplifier 6 corresponds to read means, and receives a signal r_out selectively output from the sensor array blocks $2_1$ to $2_n$ (e.g., in the sensor array block $2_1$, a signal r_out output from the RAM $17_1$ via the buffer $13_1$ with a selection signal), and pixel signals s_out selectively output from the sensor array blocks $2_1$ to $2_n$ (e.g., in the sensor array block $2_1$, pixel signals s_out output from the memory $14_1$ via the analog switch $12_1$). The read amplifier 6 multiplies each pixel signal s_out by a gain according to the signal r_out, and outputs it as a signal Vout.

[0065]

The respective building units of the photoelectric conversion device 100 have been described.

The controller 1 which performs the operation control of the entire photoelectric conversion device 100, especially, the charge accumulation control of the sensor array blocks $2_1$ to $2_n$, will be described in

detail below.

Note that a control method according to the present invention is executed by the controller 1.

[0066]

For example, the program memory 18 of the controller 1 stores processing programs according to the flow charts shown in Figs. 3 to 5, and when these processing programs are read out and executed by the controller 1, the following charge accumulation control is done.

[0067]

(Main Processing: Fig. 3)

The controller 1 performs the following reset processing first (step S101).

[0068]

(Main Processing - Reset Processing: Fig. 4)

The controller 1 outputs a reset signal rst to the sensors $16_1$ to $16_n$ of the sensor array blocks $2_1$ to $2_n$ (step S201).

In response to this signal, charges on the sensors $16_1$ to $16_n$ of the sensor array blocks $2_1$ to $2_n$ are cleared, thus starting actual charge accumulation.

[0069]

The controller 1 then sets a register value r_sel of its internal register (not shown) for sensor array block selection (region selection) at an initial value "1" (step S202).

[0070]

The controller 1 outputs a signal max_level to the level output circuit 3 (step S203).

In response to this signal, the count value (signal c_out) of the counter 28 in the level output circuit 3 is set at "3".

[0071]

The controller 1 outputs a signal W_ram to the buffer with a selection signal, and outputs signals ltcR_x (x = 1 to n) to the RAM $17_x$ of the sensor array block $2_x$ selected according to the register value r_sel (step S204).

Note that the register value r_sel indicates the sensor array block (region) to be selected, and "x = r_sel".

With this signal, the RAM $17_x$ in the sensor array block $2_x$ (x = r_sel = 1 to n) corresponding to the register value r_sel stores the output signal c_out (count value = "3") from the level output circuit 3.

[0072]

The controller 1 checks if the register value r_sel is "n", i.e., if "3" is written in the RAMs $17_1$ to $17_n$ in the sensor array blocks $2_1$ to $2_n$ corresponding to all the regions 1 to n (step S205).

[0073]

If the end of write is not determined in step S205, the controller 1 increments the register value

r_sel (step S206), and the flow returns to step S204 to repeat the subsequent processes.

In this way, "3" is written in the RAMs $17_1$ to $17_n$ in the sensor blocks $2_1$ to $2_n$ corresponding to all the regions 1 to n.

After that, the control returns to the main processing shown in Fig. 3 (step S207).

[0074]

(Main Processing: Fig. 3)

Upon completion of the reset processing in step S101, the controller 1 then sets its internal timer (not shown) at an initial value "0" (timer = 0), thereby starting time measurement of charge accumulation (step S102).

[0075]

The controller 1 sets the register value r_sel of its internal register used in the aforementioned reset processing at an initial value "1" (step S103).

[0076]

The controller 1 then checks if the timer value timer of the internal timer has exceeded a maximum accumulation time Etime (step S104).

If "timer $\geq$ Etime", the flow advances to step S109 (to be described later).

[0077]

On the other hand, if "timer < Etime" in step S104, the controller 1 outputs a signal psel_x to the

analog switch $12_x$ in the sensor array block $2_x$ selected in accordance with the register value r_sel.

Also, the controller 1 outputs a signal rsel_x to the buffer $13_x$ with a selection signal of in the sensor array block $2_x$, and a signal sel_level to the level output circuit 3 (step S104).

In response to these signals, the output signal (maximum accumulated charge amount) of the peak detection circuit $15_x$ in the sensor array block $2_x$ is output to one input terminal ("+" terminal) of the comparator 5 as a signal p_out via the analog switch $12_x$.

The output from the RAM $17_x$ in the sensor array block $2_x$ is supplied as a signal r_out to the read amplifier 6 and level output circuit 3 via the buffer $13_x$ with a selection signal. In the level output circuit 3, the selector 27 selects the signal r_out, and that selected signal is directly supplied to the decoder 26 as a signal sel_out. The decoder 26 selects one of the four level values level1.3, level1.2, level1.1, and level1.0 in accordance with the signal sel_out. The selected level value is output as a signal c_level via the amplifier 25.

[0078]

Subsequently, the controller 1 checks if the output signal comp from the comparator 5 is "1", i.e., if the output signal (level value) c_level of the level

output circuit 3 is larger than the output signal p_out of the peak detection circuit $15_x$ in the sensor array block $2_x$ (step S106).

If "comp = 1", the flow advances to step S109 (to be described later).

[0079]

On the other hand, if "comp $\neq$ 1" in step S106, the controller 1 checks if the timer value timer of the internal timer reaches an intermediate accumulation time Htime (step S107).

If "timer $\neq$ Htime", the flow advances to step S110 (to be described later).

Note that "timer = Htime" means that the timer value timer of the internal timer roughly equals the intermediate accumulation time Htime. The time required for completing gain determination (to be described later) for all the regions can be sufficiently determined to be "timer = Htime".

[0080]

If "timer = Htime" in step S107, the controller 1 executes the following gain determination (step S108).

[0081]

(Main Processing - Gain Determination: Fig. 5)

The controller 1 outputs a signal rst_level to the level output circuit 3 (step S301).

In response to this signal, in the level output circuit 3, the count value of the counter 28 is cleared

to "0", and its output signal c_out = "0" is output.

[0082]

The controller 1 checks if the output signal comp of the comparator 5 is "1", i.e., if the output signal c_level of the level output circuit 3 is larger than the output signal p_out of the peak detection circuit $15_x$ in the sensor array block $2_x$ (step S302).

As a result of checking, if "comp ≠ 1", the flow advances to step S305 (to be described later).

[0083]

On the other hand, if "comp = 1" in step S302, the controller 1 checks if the output signal c_out from the level output circuit 3 is "3" (step S303).

If "c_out = 3", the flow advances to step S305 (to be described later).

[0084]

If "c_out ≠ 3" in step S303, the controller 1 outputs a signal G_up to the level output circuit 3 (step S304).

In response to this signal, in the level output circuit 3, the count value (c_out) of the counter 28 is incremented.

After that, the flow returns to step S302 to repeat the subsequent processes.

[0085]

If "comp ≠ 1" in step S302, or if "c_out = 3" in step S303, the controller 1 outputs a signal W_ram to

the buffer 4 with a selection signal, and signals ltcR_x to the RAM $17_x$ in the sensor array block $2_x$ (step S305).

In response to these signals, the RAM $17_x$ in the sensor array block $2_x$ stores the output signal c_out of the level output circuit 3.

After this processing, the control returns to the main processing shown in Fig. 3 (step S306).

[0086]

As described above, in this gain determination, the gain of the read amplifier 6, i.e., the charge accumulation end level (the output signal c_out of the level output circuit 3) is determined on the basis of the output signal p_out from the peak detection circuit $15_x$ in the sensor array block $2_x$, and the count value (c_out) corresponding to the determined level is written in the RAM $17_x$ in the sensor array block $2_x$.

Since this count value (c_out), i.e., the count value of the counter 28 of the level output circuit 3 is counted up one by one from the initial value "0", the output signal c_level of the level output circuit 3 gradually increases from "level1.0" to "level1.1", from "level1.1" to "level1.2", and so on.

[0087]

Hence, when "comp = 1" is not detected at "level1.0", since the output signal p_out from the peak detection circuit $15_x$ is lower than "level1.0", the

charge accumulation end level is determined to be "level1.0", and the count value (c_out = 0) corresponding to that level is written in the RAM $17_x$.

After "comp = 1" is detected at "level1.0", when "comp = 1" is not detected at "level1.1", since the output signal p_out of the peak detection circuit $15_x$ falls within the range between "level1.0" and "level1.1", the charge accumulation end level is determined to be "level1.1", and the count value (c_out = 1) corresponding to that level is written in the RAM $17_x$.

Similarly, when the output signal p_out falls within the range between "level1.1" and "level1.2", "level1.2" is determined. When the output signal p_out falls within the range between "level1.2" and "level1.3", "level1.3" is determined. In each case, the corresponding count value (c_out = 2 or 3) is written.

[0088]

(Main Processing: Fig. 3)

On the other hand, if "timer ≧ Etime" (the timer value timer of the internal timer has exceeded the maximum accumulation time Etime) in step S104, or if "comp = 1" (the level value c_level has exceeded the output signal p_out of the peak detection circuit $15_x$ in the sensor array block $2_x$) in step S106, the controller determines the end of charge accumulation,

and outputs a signal trans indicating this to the sensor $16_x$ in the sensor array block $2_x$ (step S109).

In response to this signal, in the sensor array block $2_x$ corresponding to the region x, charges accumulated on the respective pixels of the sensor $16_x$ are transferred as pixel signals to the memory $14_x$, thus ending charge accumulation on the sensor $16_x$.

[0089]

After the processing in step S109, or after the aforementioned gain determination (step S108), or if "timer = Htime" is not detected (the timer value timer of the internal timer does not exceed the intermediate accumulation time Htime), the controller 1 checks if the register value r_sel of the internal register is "n", i.e., if the processes in step S104 to S109 are complete for the sensor array blocks $2_1$ to $2_n$ corresponding to all the regions 1 to n (step S110).

[0090]

If "r_sel = n" in step S110, the controller 1 resets the register value r_sel of the internal register to "1" to select the sensor array block $2_1$ corresponding to the initial region 1, and repeats the processes from step S104.

On the other hand, if "r_sel ≠ n", the controller 1 increments the register value r_sel of the internal register to select the next sensor array block $2_{x+1}$ corresponding to the next region (x+1) and repeats

the processes from step S104.

[0091]

The charge accumulation control on the sensor array blocks $2_1$ to $2_n$ by the controller 1 has been described.

The operations of the sensor array blocks $2_1$ to $2_n$ by the aforementioned charge accumulation control will be explained below with reference to Figs. 6(A) and 6(B).

[0092]

In Figs. 6(A) and 6(B), the abscissa plots the charge accumulation time, and the ordinate plots the output signal c_level of the level output circuit 3, and the output signal p_out of the peak detection circuit $15_x$ in the sensor array block $2_x$.

Fig. 6(A) shows a case wherein the object is relatively bright, and the peak output of each pixel signal, i.e., the output signal p_out of the peak detection circuit $15_x$ of the sensor array block $2_x$ rises quickly. Fig. 6(B) shows, contrary to Fig. 6(A), a case wherein the object is relatively dark, and the peak output of each pixel signal rises slowly.

[0093]

(Case of Fig. 6(A))

When charge accumulation is started, since "3" is written in the RAMs $17_1$ to $17_n$ in the sensor array blocks $2_1$ to $2_n$ corresponding to all the regions 1 to

n, the output signal c_level of the level output circuit 3 indicates "level1.3".

When the output signal p_out from the peak detection circuit $15_x$ in the sensor array block $2_x$ corresponding to a certain region x has reached this "level1.3" (point P_A), the charge accumulation in that sensor array block $2_x$ ends.

Note that the same applies to the sensor array blocks corresponding to other regions.

[0094]

(Case of Fig. 6(B))

When charge accumulation is started, since "3" is written in the RAMs $17_1$ to $17_n$ in the sensor array blocks $2_1$ to $2_n$ corresponding to all the regions 1 to n, the output signal c_level of the level output circuit 3 indicates "level1.3".

In this case, since the peak output (p_out) of each pixel signal rises slowly, when the charge accumulation time (the timer value timer of the internal timer) has reached the intermediate accumulation time Htime (point P_B1), the gain determination (step S108) shown in Fig. 5 is executed to determine the charge accumulation end level (c_level) for the sensor array blocks $2_1$ to $2_n$ corresponding to regions 1 to n.

Referring to Fig. 6(B), since the output signal p_out from the peak detection circuit $15_x$ in the sensor

array block $2_x$ corresponding to a certain region x falls within the range between "level1.1" and "level1.2", c_level is determined to be "level1.2" for the sensor array block $2_x$, and this information ("c_out = 2" in this case) is written in the RAM $17_x$. When the output signal p_out from the peak detection circuit $15_x$ has reached "level1.2" (point P_B2), the charge accumulation in that sensor array block $2_x$ ends.

Note that the charge accumulation end level is determined in each of the sensor array blocks corresponding to regions other than region x, and that information is written in the corresponding RAM. When the peak output has reached the determined charge accumulation completion level, the charge accumulation in that sensor array block ends.

[0095]

As described above, according to this embodiment, since information associated with charge accumulation (in this case, the value (c_out) corresponding to the charge accumulation end level (c_level)) is written in the RAMs $17_1$ to $17_n$ in the sensor array blocks $2_1$ to $2_n$ corresponding to all the regions 1 to n, charge accumulation control of the sensor array blocks $2_1$ to $2_n$ corresponding to regions 1 to n can be independently made.

In addition, since operations such as count-up operation and the like are not done immediately after

the beginning of charge accumulation even for a high-luminance object, the image signal of the object can be prevented from exceeding the dynamic range, and the image is never distorted.

Hence, an accurate photoelectric conversion device 100 which can always appropriately perform charge accumulation control without increasing the circuit scale even when the number of distance measurement points of multi-point AF is increased, can be provided.

[0096]

(2) Second Embodiment

In this embodiment, for example, in the photoelectric conversion device 100 in the first embodiment described above, read control of pixel signals in the read amplifier 6 is performed as follows.

[0097]

The program memory 18 of the controller 1 pre-stores a processing program according to the flow chart shown in Fig. 7, and when this processing program is read out and executed by the controller 1, the following read control is done.

[0098]

The controller 1 selects a region from which pixel signals are to be read (in this case, a region x (x = 1 to n), and stores a value (= x) corresponding to

the region x in its internal register. The controller 1 then outputs a signal sel_x to the analog switch $11_x$ in the sensor array block $2_x$.

In this way, in the sensor array block $2_x$, pixel signals s_out held in the memory $14_x$ are ready to be sequentially output to the input terminal of the read amplifier 6 via the analog switch $11_x$.

Also, the controller 1 outputs a signal psel_x to the analog switch $12_x$ in the sensor array block $2_x$.

In response to this signal, in the sensor array block $2_x$, the output signal p_out from the peak detection circuit $15_x$ is output to one input terminal ("+" terminal) of the comparator 5 via the analog switch $12_x$ (step S401).

[0099]

The controller 1 then executes the gain determination shown in Fig. 5.

In this fashion, the level (the output signal c_level of the level output circuit 3) is determined on the basis of the output signal p_out from the peak detection circuit $15_x$ in the sensor array block $2_x$, and the count value (c_out) corresponding to the determined level is written in the RAM $17_x$ in the sensor array block $2_x$ (step S402).

[0100]

The controller 1 outputs a signal shift to the memory $14_x$ in the sensor array block $2_x$.

In response to this signal, the pixel signals s_out held in the memory $14_x$ are sequentially output to the input terminal of the read amplifier 6 via the analog switch $11_x$.

Also, the controller 1 outputs a signal rsel_x to the buffer $13_x$ in the sensor array block $2_x$.

As a result, the value (c_out) written in the RAM $17_x$ is read out as a signal Ro, and is output as a signal r_out to the read amplifier 6 via the buffer $13_x$ with a selection signal.

Hence, the read amplifier 6 multiplies each pixel signal s_out from the memory $14_x$ by a gain based on the signal r_out, e.g., a gain selected from a plurality of preset gains in accordance with the signal r_out, and outputs it from the output terminal Vout (step S403).

[0101]

To restate, according to this embodiment, the gain determination (level determination upon completion of charge accumulation) shown in Fig. 5 is performed immediately before pixel signals are read out. For this reason, even when gain determination cannot be done during charge accumulation by setting a constant charge accumulation time in, e.g., moving body predictive AF, that gain determination is done immediately before pixel signals are read out, and the pixel signals are read out with the gain obtained as the gain determination result. Hence, an accurate

photoelectric conversion device 100 which can always appropriately read out pixel signals can be provided.

[0102]

Note that the present invention is not limited to the aforementioned AF camera, but may be applied to various other apparatuses having a focus detection function.

[0103]

In the first and second embodiments described above, the output from the peak detection circuit is used in gain determination. However, the present invention is not limited to this. For example, the peak and bottom values may be detected, and a so-called peak-bottom signal obtained by calculating the difference between the peak and bottom values may be used.

[0104]

In the second embodiment, the first embodiment may be modified to do gain determination immediately before a read when gain determination is disturbed for some reasons.

Note that "some reasons" are, for example:

・the maximum accumulation time Etime is short;

・when gain determination is made using a circuit for outputting a peak-bottom difference in place of the peak detection circuit, operation for ending accumulation is made since the peak output has exceeded

a predetermined level;

and so forth.

[0105]

The sensors $16_1$ to $16_n$ in the sensor array blocks $2_1$ to $2_n$ may use any kinds of sensors such as CCDs, CMOS sensors, and the like.

[0106]

Also, the RAMs $17_1$ to $17_n$ in the sensor array blocks $2_1$ to $2_n$ may use either digital memories or analog memories.

[0107]

The objects of the present invention are also achieved by supplying a storage medium, which records a program code of a software program that can realize the functions of the host and terminal of the above-mentioned first and second embodiments to a system or apparatus, and reading out and executing the program code stored in the storage medium by a computer (or a CPU or MPU) of the system or apparatus.

In this case, the program code itself read out from the storage medium realizes the functions of the above-mentioned embodiments, and the storage medium which stores the program code constitutes the present invention.

[0108]

As the storage medium for supplying the program code, for example, a floppy disk, hard disk, optical

disk, magneto-optical disk, CD-ROM, CD-R, magnetic tape, nonvolatile memory card, ROM, and the like may be used.

[0109]

The functions of the above-mentioned first and second embodiments may be realized not only by executing the readout program code by the computer but also by some or all of actual processing operations executed by an OS or the like running on the computer on the basis of an instruction of the program code.

[0110]

Furthermore, the functions of the above-mentioned first and second embodiments may be realized by some or all of actual processing operations executed by a CPU or the like arranged in a function extension board or a function extension unit, which is inserted in or connected to the computer, after the program code read out from the storage medium is written in a memory of the extension board or unit.

[0111]

[Effects of the Invention]

As has been described above, according to the present invention, storage means (for example, a memory which can read and write information) corresponding to a photoelectric conversion element is used, and charge accumulation in the photoelectric conversion (start and end of charge accumulation, and the like), and the

amplification factor (gain) upon reading out pixel signals are controlled on the basis of control information read out from the storage means. Hence, appropriate charge accumulation can always be done irrespective of the luminance levels of objects, and pixel signals can always be read out with an appropriate gain.

Especially, even when the number of distance measurement points is large in, e.g., a multi-point auto-focus camera, appropriate charge accumulation can always be done, and pixel signals can always be read out with an appropriate gain. In addition, the pixel signals can be read out by effectively using the dynamic range without impairing it. Hence, a low-cost device which can realize accurate auto-focus without increasing its circuit scale can be provided.

When the photoelectric conversion element and the corresponding storage means are integrally formed on a single substrate, control efficiency can be improved. Even when the number of distance measurement points is large, a lower-cost device which can improve operability without increasing the circuit scale can be provided.

[Brief Description of the Drawings]

[Fig. 1]

Fig. 1 is a block diagram showing the arrangement of a photoelectric conversion device to which a

photoelectric conversion device according to the present invention is applied in the first embodiment.

[Fig. 2]

Fig. 2 is a block diagram showing the arrangement of a level output circuit of the photoelectric conversion device.

[Fig. 3]

Fig. 3 is a flow chart for explaining a charge accumulation control program (main processing) executed by a controller of the photoelectric conversion device.

[Fig. 4]

Fig. 4 is a flow chart for explaining a reset program in the charge accumulation control program.

[Fig. 5]

Fig. 5 is a flow chart for explaining a gain determination program in the charge accumulation control program.

[Fig. 6]

Fig. 6 shows graphs for schematically explaining the charge accumulation in the photoelectric conversion device.

[Fig. 7]

Fig. 7 is a flow chart for explaining a read control program of pixel signals executed by the controller of the photoelectric conversion device in the second embodiment.

[Fig. 8]

Fig. 8 is a block diagram showing the arrangement of a conventional photoelectric conversion device.

[Fig. 9]

Fig. 9 is a flow chart for explaining conventional charge accumulation control.

[Fig. 10]

Fig. 10 shows graphs for schematically explaining the charge accumulation in the conventional photoelectric conversion device.

[Description of the Reference Numerals]

| | |
|---|---|
| 100 | photoelectric conversion device |
| 1 | controller |
| $2_1$ - $2_n$ | sensor array block |
| 3 | level output circuit |
| 4 | buffer with selection signal |
| 5 | comparator |
| 6 | read amplifier |
| $11_1$ | analog switch |
| $12_1$ | analog switch |
| $13_1$ | buffer with selection signal |
| $14_1$ | memory |
| $15_1$ | peak detection circuit |
| $16_1$ | sensor |
| $17_1$ | RAM |
| 18 | program memory |

[Type of the Document] Abstract

[Abstract]

[Problem] There is provided a photoelectric conversion device which can always perform appropriate charge accumulation control independently of the luminance levels of objects to read pixel signals by effectively using the dynamic range, can attain accurate auto-focus, and can realize them without increasing the circuit scale and cost.

[Solving Means] A storage means $17_x$ corresponding to a photoelectric conversion element $16_x$ is used, and a control means 1 controls charge accumulation in the photoelectric conversion element $16_x$ (start and end of charge accumulation, and the like) on the basis of control information read out from the storage means $17_x$.

[Selected Drawing] Fig. 1